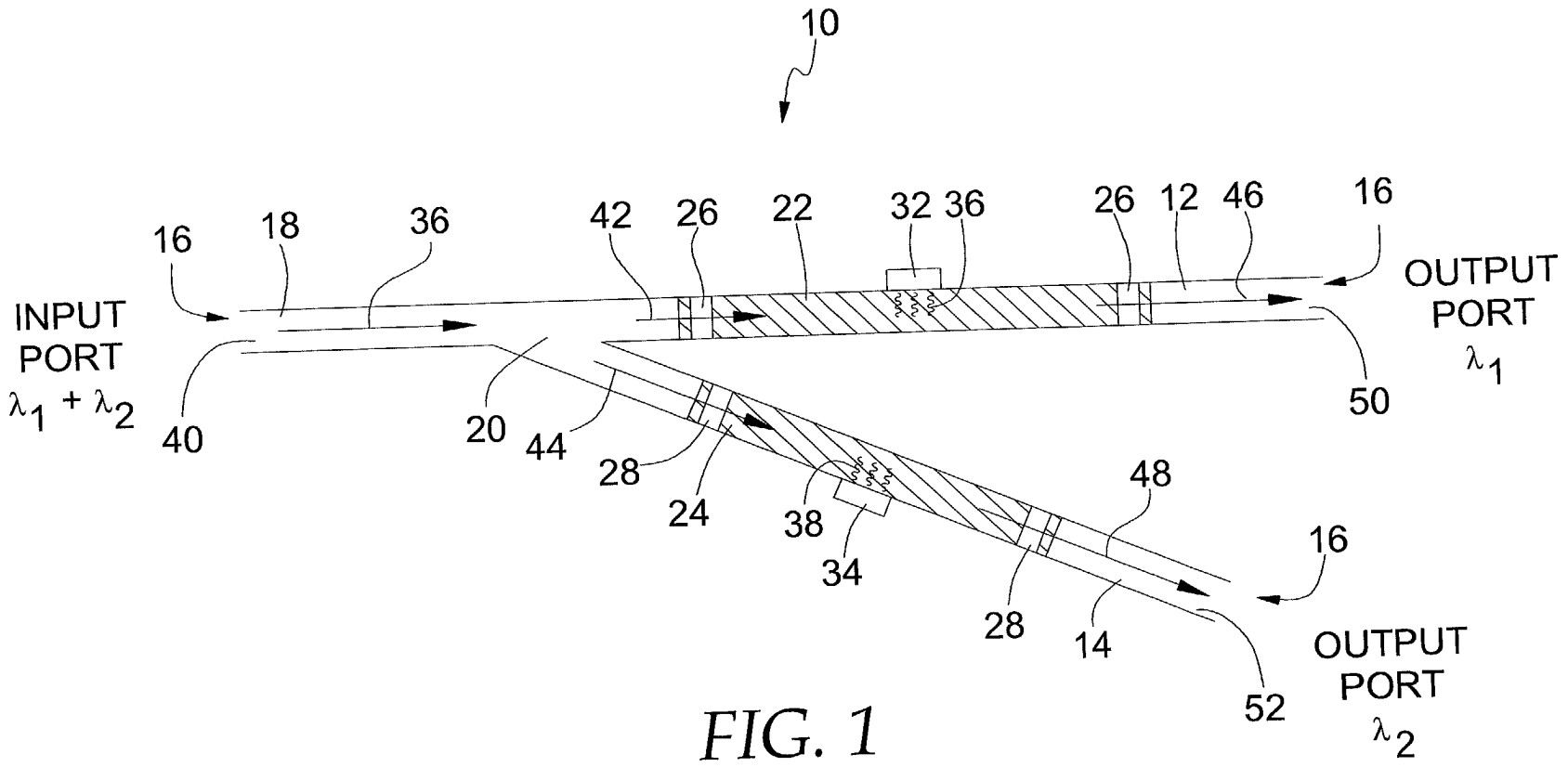
10
16
18
36
42
26
22
32
36
26
12
46
16
INPUT PORT $\lambda_1 + \lambda_2$
OUTPUT PORT λ_1
40
20
44
28
24
38
34
48
16
28
14
52
50
OUTPUT PORT λ_2

FIG. 1

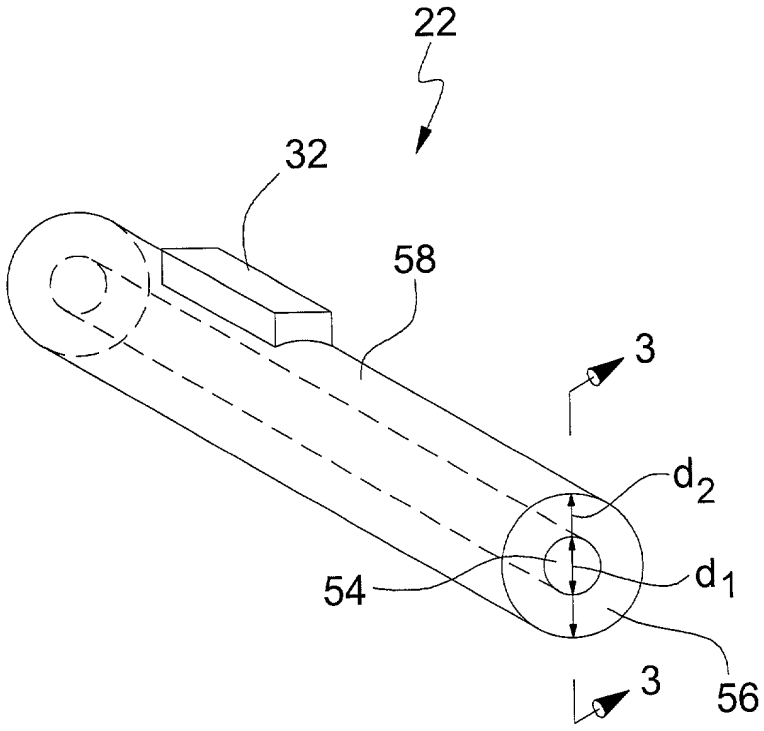

FIG. 2

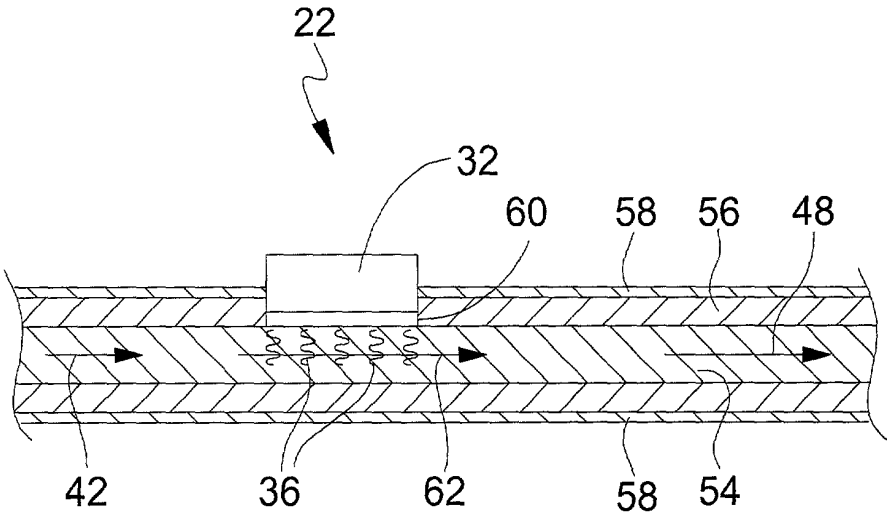

FIG. 3

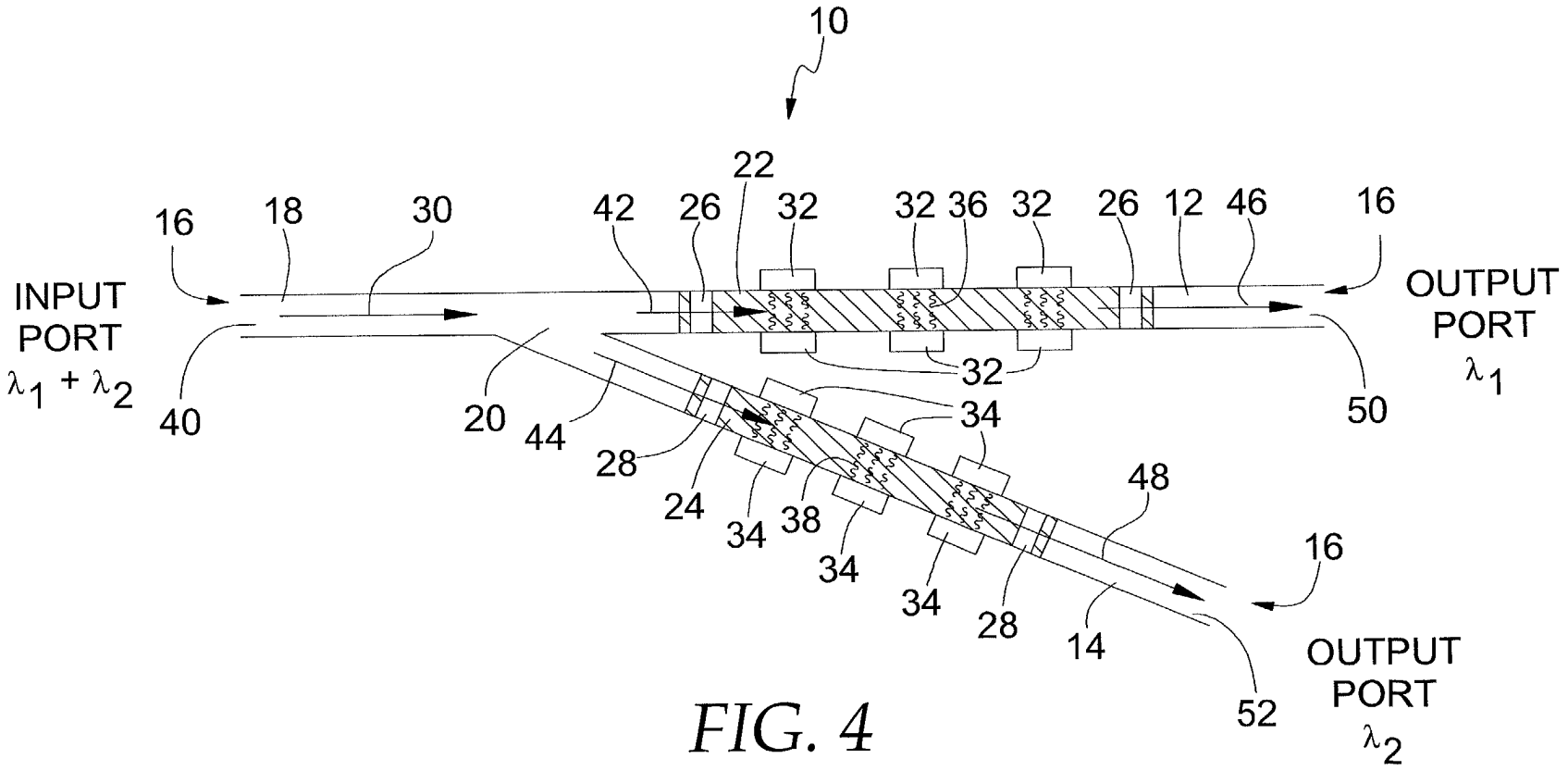
10
22
16
18
30
42
26
32
32
36
32
26
12
46
16
INPUT
PORT
$\lambda_1 + \lambda_2$
OUTPUT
PORT
λ_1
40
20
44
28
24
34
38
34
34
34
28
14
48
16
50
32
34
52
OUTPUT
PORT
λ_2

FIG. 4

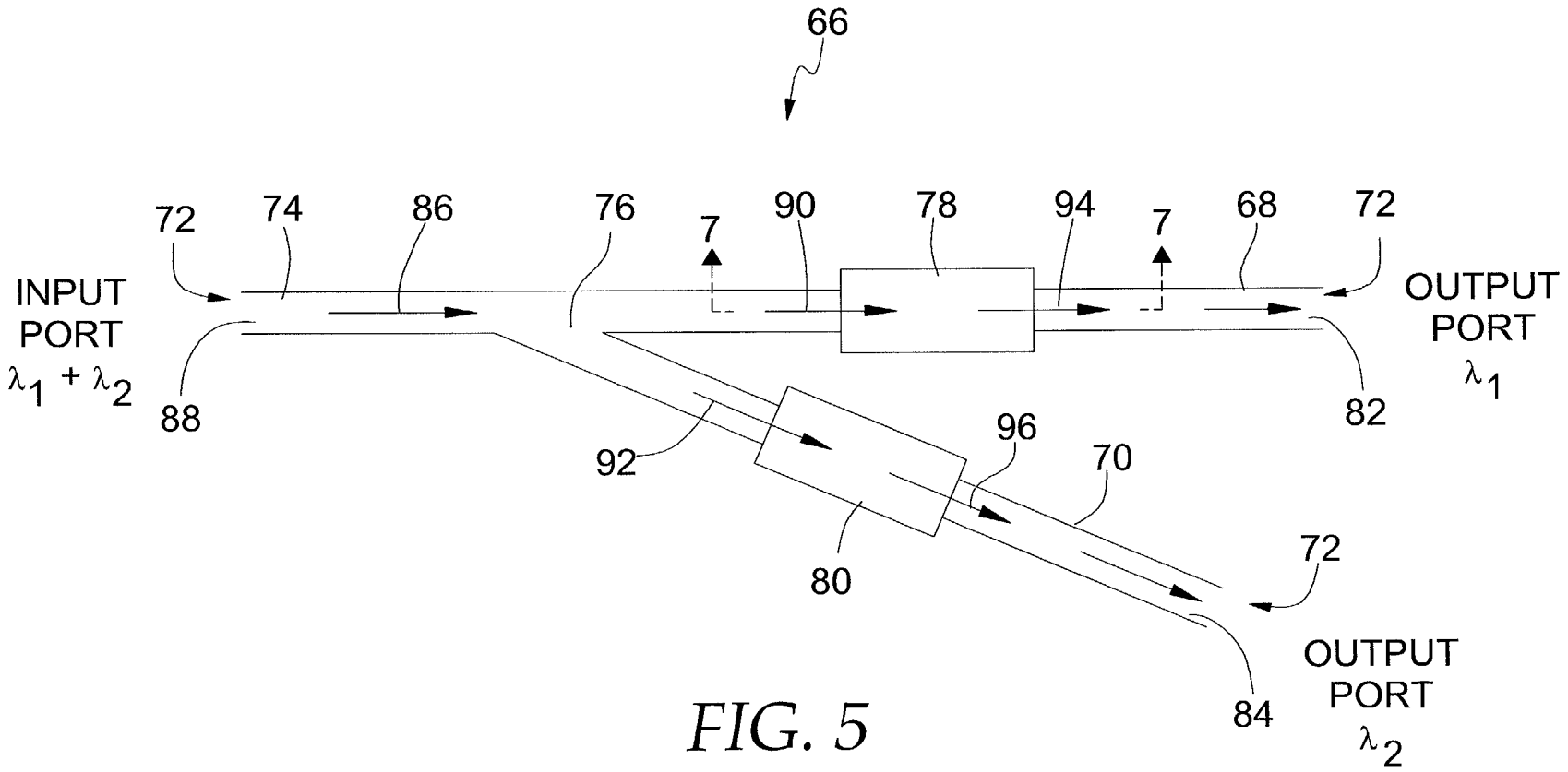

FIG. 5

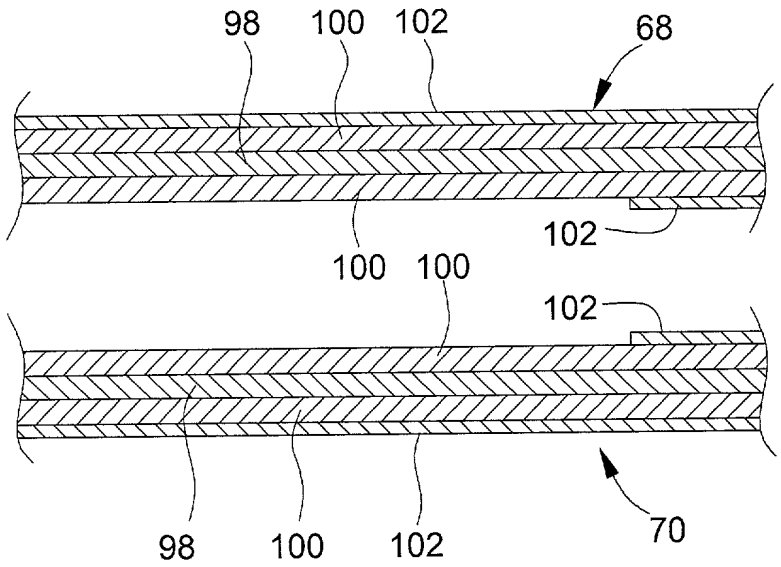
98
100
102
68
102
100
100
102
98
100
102
70

FIG. 6A

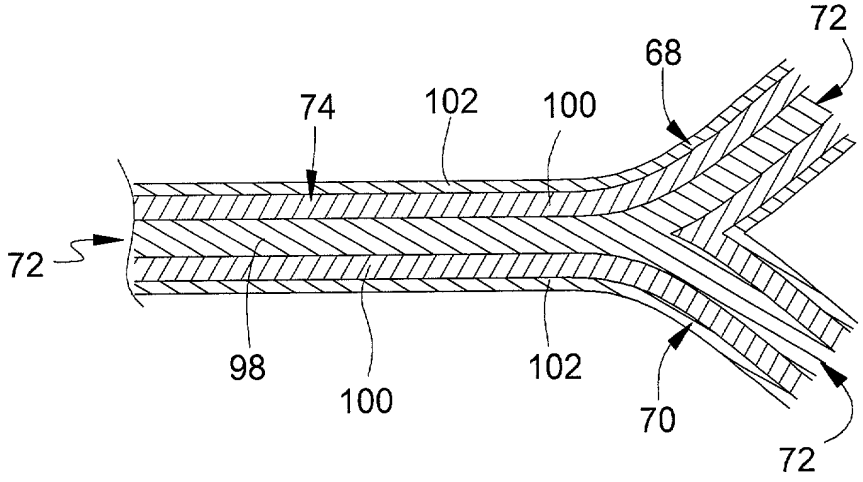
72
68
74
102
100
72
98
100
102
70
72

FIG. 6B

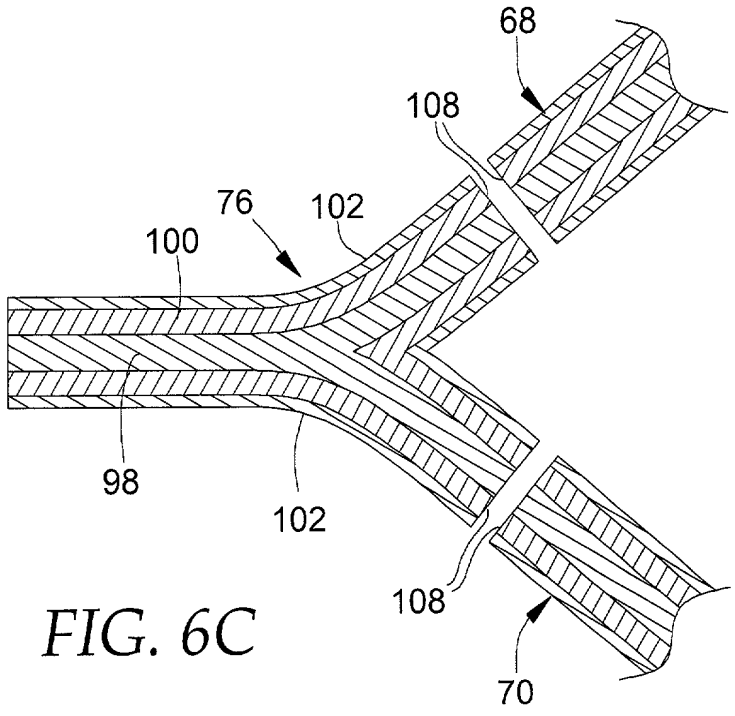
68
108
76
102
100
98
102
108
70

FIG. 6C

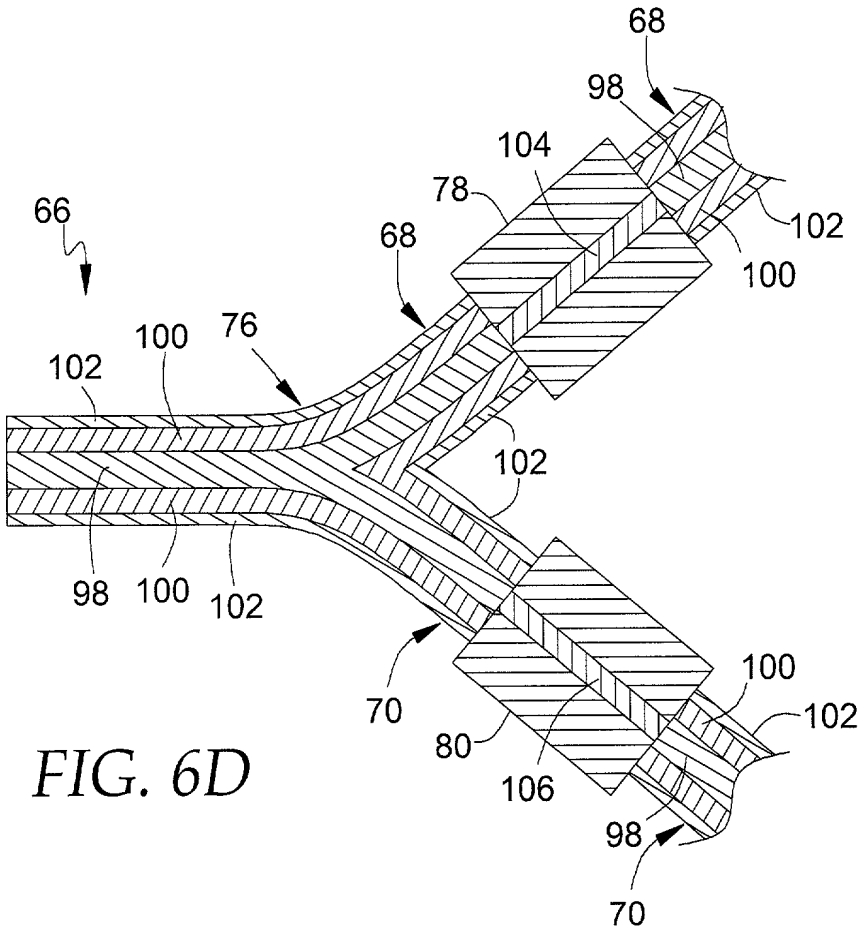
68
98
104
78
66
68
102
100
76
100
102
102
98
100
102
70
100
102
80
106
98
70

FIG. 6D

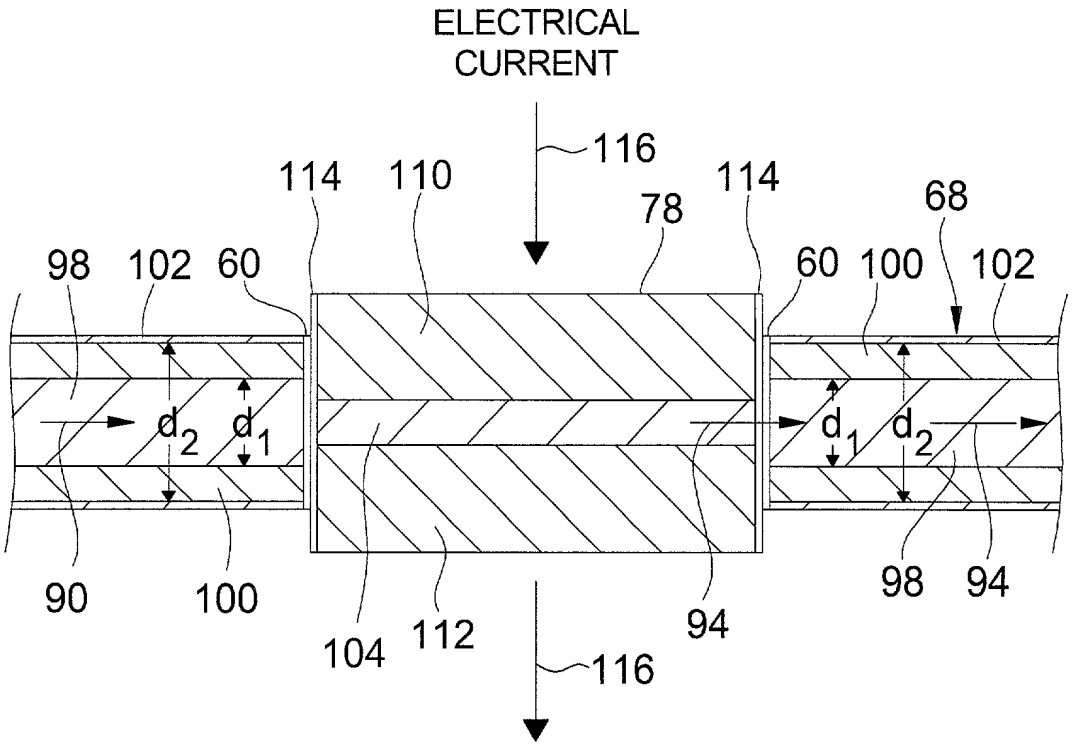
ELECTRICAL
CURRENT
116
114
110
78
114
68
98
102
60
60
100
102
d_2
d_1
d_1
d_2
90
100
104
112
94
98
94
116

FIG. 7

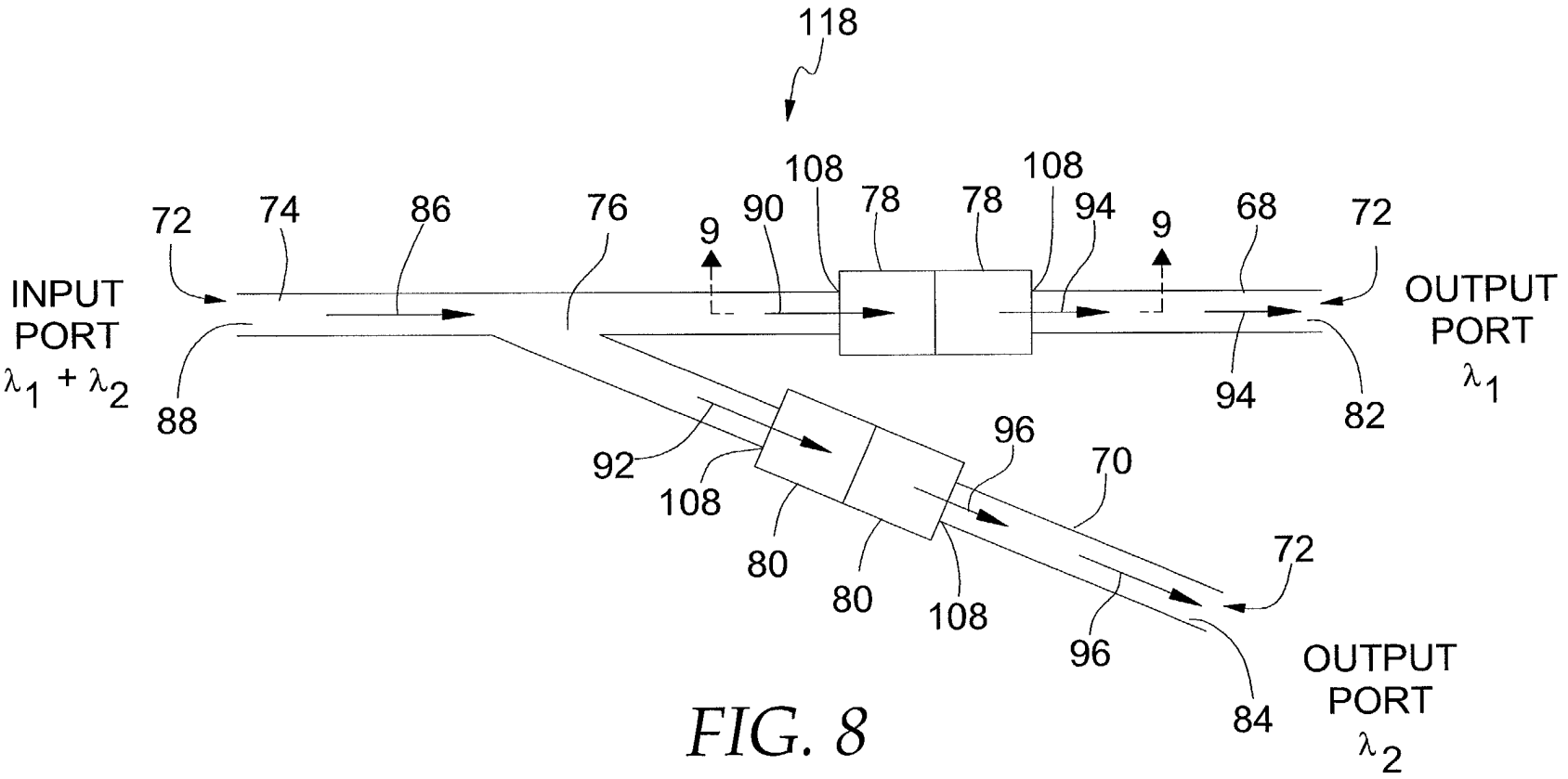
118
108
108
72
74
86
76
9
90
78
78
94
9
68
72
INPUT
PORT
$\lambda_1 + \lambda_2$
OUTPUT
PORT
λ_1
88
94
82
96
92
70
108
72
80
80
108
96
OUTPUT
PORT
λ_2
84

FIG. 8

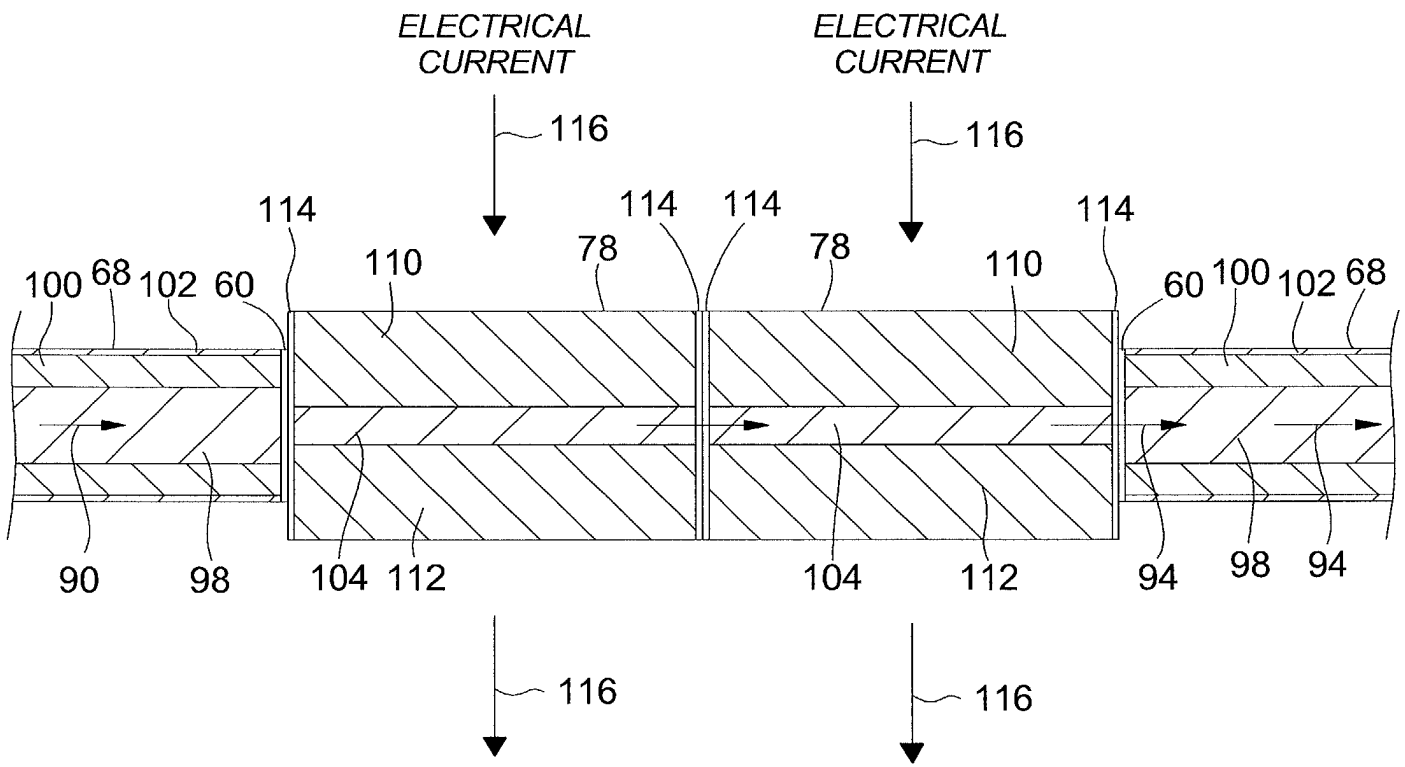

FIG. 9

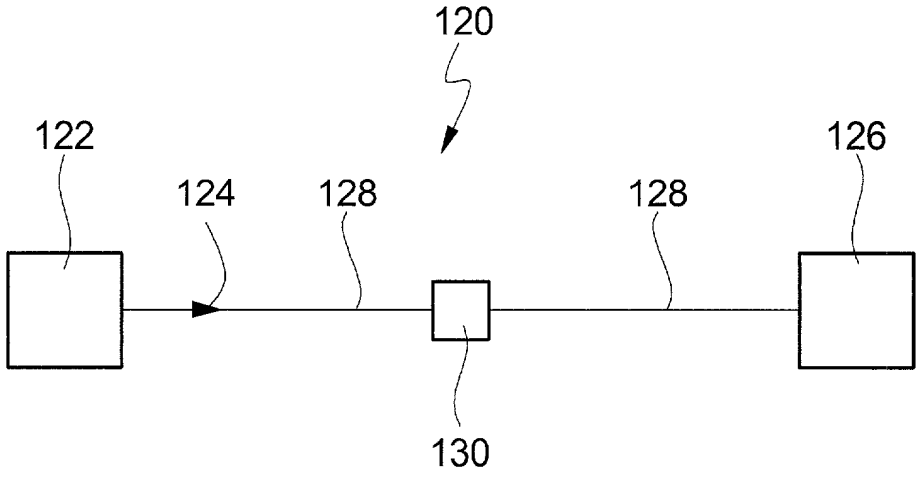

FIG. 10